INFORMATION DISCLOSURE CITATION
(Use several sheets if necessary)

Docket Number (Optional)	Application Number
BUR920010167US1	09/683,733

Applicant(s)
Aday et al.

Filing Date	Group Art Unit
02/07/02	

U.S. PATENT DOCUMENTS

*EXAMINER INITIAL	REF	DOCUMENT NUMBER	DATE	NAME	CLASS	SUBCLASS	FILING DATE IF APPROPRIATE
✓		US20010023418A1	09/2001	Suzuki et al.	705	400	
✓		US 6,249,776 B1	06/2001	Bajuk et al.	705	400	
✓		5,960,417	09/1999	Pan et al.	705	400	

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FOREIGN PATENT DOCUMENTS

	REF	DOCUMENT NUMBER	DATE	COUNTRY	CLASS	SUBCLASS	Translation YES	NO

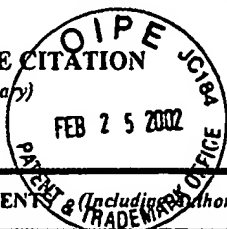### OTHER DOCUMENTS *(Including Author, Title, Date, Pertinent Pages, Etc.)*

✓	P. K. Nag, W. Maly, and H. J. Jacobs, "Simulation of Yield/Cost Learning Curves with Y4," IEEE Transactions on Semiconductor Manufacturing, vol. 10, no. 2, pp. 256 - 266, May 1997.
✓	R. Ross, J. Bailey, N. Atchison, and M. Effron, "A Comprehensive Sequential Yield Analysis Methodology and the Financial Payback for Higher Yields," 1999 IEEE/SEMI Advanced Semiconductor Manufacturing Conference, pp. 80-86, 1999.

EXAMINER *Freda Nelson*	DATE CONSIDERED *June 8, 2006*

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Docket Number (Optional) BUR920010167US1	Application Number 09/683,733
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(initialed)		C. A. Moritz, D. Yeung, and A. Agarwal, "SimpleFit: A Framework for Analyzing Design Trade-Offs in Raw Architectures," IEEE Transactions on Parallel and Distributed Systems, vol. 12, no. 7, pp. 730-742, July 2001
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